

REMARKS

Claims 1 and 2 have been amended to more closely conform to U.S. claiming practice, and the specification has been amended to employ more idiomatic English. No new matter has been entered by any of the foregoing amendments.

The allowance of claims 2, 4, 6 and 8 is noted with thanks.

Turning to the art rejections, the rejection of claim 1 under 35 USC §102(b) as anticipated by Hirai et al. (Japanese Publication No. 10-293559) is in error. Hirai et al. is discussed in Applicants' specification beginning at page 1, line 22, and its deficiencies noted. Other than teaching a charge reusing circuit generally employing switches and capacitors, Hirai et al. supplies none of the teachings of the claimed combination as set forth in claim 1. Thus, claim 1 cannot be achieved nor rendered obvious by Hirai et al.

The rejection of claims 3, 5, and 7 under 35 USC §103(a) as being unpatentable over Hirai in view of Harada (Japanese Publication No. 2002-041003) is also in error. Claims 3, 5, and 7 depend, directly or indirectly, on independent claim 1. The deficiencies of Hirai et al. vis-à-vis Applicants' claim 1 are discussed above. Harada does not teach a charge collection and resupply circuit according to the claims. Thus, no combination of Hirai et al. and Harada can achieve nor render obvious independent claim 1 and any claims which depend therefrom.

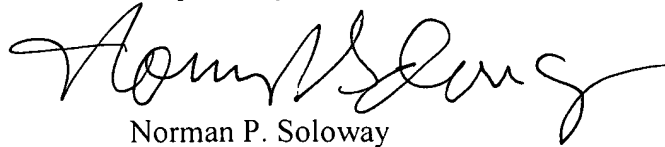
Having dealt with all the objections raised by the Examiner, the Application is believed to be in order for allowance. Early and favorable action is respectfully requested.

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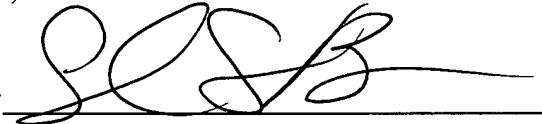
Respectfully submitted,



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